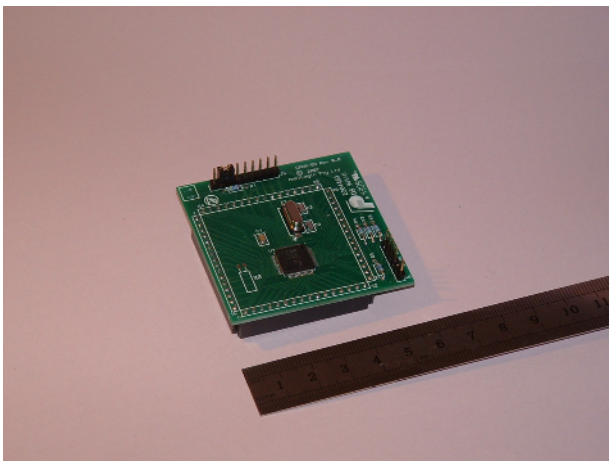
CPDA-99 Embedded
Digital + Analog Processor

A Much Better Idea : Logical : Unique

AmbiLogique

Electronic Controllers



Features:-

42 Inputs and Outputs:

- 16 - Digital Inputs
- 6 - 0 to 2.5 V Analog Inputs
- 15 - Digital Outputs
- 3 - PWM Outputs
- 2 - 0 to 2.5V Analog Outputs

3 Medium-Speed (1kHz) counters

- 2 up-count
- 1 quadrature up/down-count

Easy Function Block Programming
Fast 16 Hz Scan Rate
Low 300 mW power consumption.

Attaches and connects to mother board via 0.1" pitch pin headers.

Built-in Serial Communication Port
8 Computer Interface Registers
All Internal Signals Viewable via Serial Port

The CPDA-99 is a programmable digital + analogue controller which is designed to be incorporated into the user's own electronic equipment. It provides a versatile and easily-programmed processor core with a stable well-proven operating system.

The operating system, programming method and facilities are identical to the AmbiLogique CPDA-01 industrial PLC. This means that control systems can be quickly programmed using a SKDA-01 Starter Kit, the control diagram developed, and the same control diagram will then run on the embedded CPDA-99 with a few adjustments to the input and output terminal address assignments.

The CPDA-99 has the following selection of inputs and outputs built in:-

- 16 digital inputs
- 6 0 to 2.5 V non-isolated analog inputs
- 15 non-isolated digital outputs
- 3 31.25 kHz PWM outputs with 256 steps of resolution
- 2 0 to 2.5 V non-isolated analog outputs

This makes a total of 42 inputs and outputs.

Connections are made via 0.1" pitch header pins arranged in a square on the parent equipment's mother board.

Please Note: Some AmbiLogique products or components may carry the "AmbiLogic" trade mark from our former Australian company.

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The CPDA-99 controller requires a 3.3 to 3.6 Vdc power supply together with a 2.500 V reference supply. All timing and clock components are on board.

Programming is carried out on a Windows ® personal computer (PC) on which the AmbiLogique design software is run. This software enables you to construct a function-block-based diagram which defines the program which the CPDA-99 will run in service.

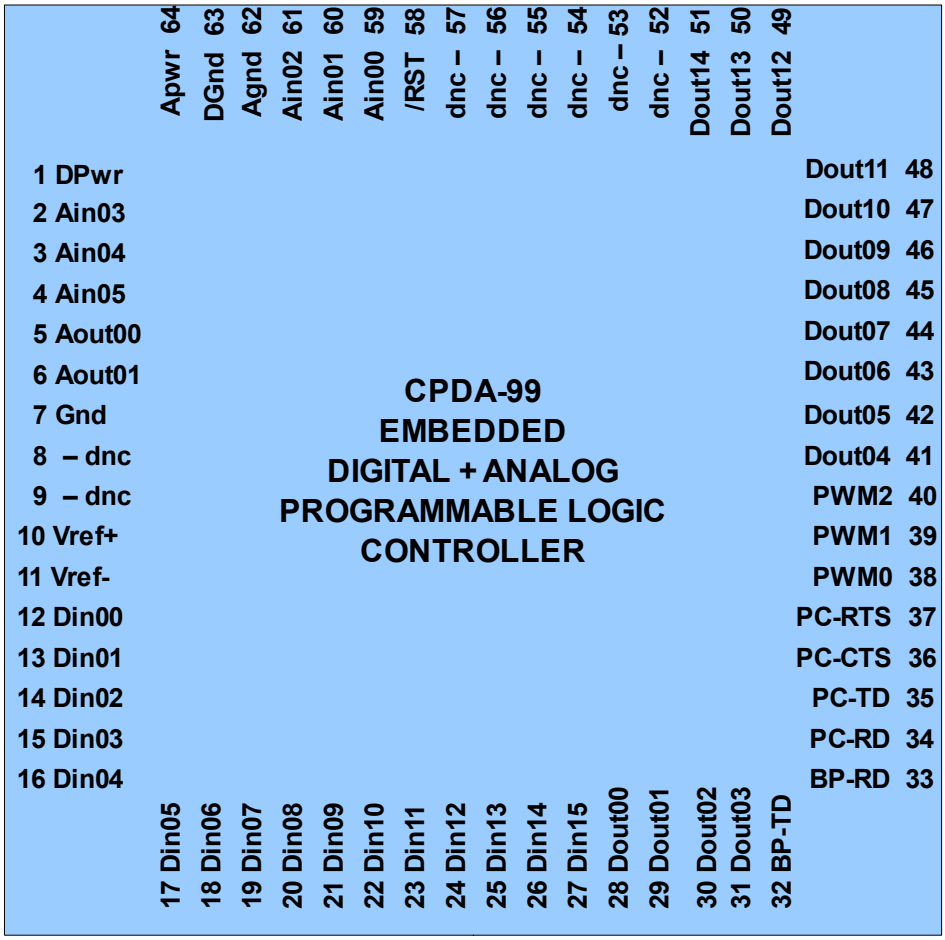
The PC is then connected to the CPDA-99 via a serial RS-232 cable with a low-level adaptor, and the compiled diagram is uploaded into the CPDA-99.

Whilst in operation, the state of the internal signals in the CPDA-99 can be displayed on the diagram on the PC screen.

Once the program has been tested, the PC can be disconnected, and the CPDA-99 will continue to operate independently.

The host computer can interact with the control diagram via 8 bidirectional registers which can be interfaced via TERMIN and TERMOUT function blocks. Both multi-bit digital and analog values can be exchanged by this means.

Connections:



Connection Diagram (See table below for the explanation of the signal names)

Connections: (continued)

Note: The Subslot, Register and Mask values are needed to map the physical inputs and outputs into the Control Diagram.

Terminal	Signal	Description	Subslot	Register	Mask
1	DPwr	+3.3 to 3.6V Digital Power			
2	Ain03	0 to 2.5V Analog Input	0	6	0
3	Ain04	0 to 2.5V Analog Input	0	7	0
4	Ain05	0 to 2.5V Analog Input	0	8	0
5	Aout00	0 to 2.5V Analog Output	0	11	0
6	Aout01	0 to 2.5V Analog Output	0	12	0
7	Gnd	Analog Ground			
8	- dnc -	Do not connect			
9	- dnc -	Do not connect			
10	Vref+	+ 2.500 Reference Voltage Input			
11	Vref-	Reference Voltage return (Gnd potential)			
12	Din00	Digital Input	0	1	1
13	Din01	Digital Input	0	1	2
14	Din02	Digital Input	0	1	4
15	Din03	Digital Input	0	1	8
16	Din04	Digital Input	0	1	16
17	Din05	Digital Input	0	1	32
18	Din06	Digital Input	0	1	64
19	Din07	Digital Input	0	1	128
20	Din08	Digital Input	0	2	1
21	Din09	Digital Input	0	2	2
22	Din10	Digital Input	0	2	4
23	Din11	Digital Input	0	2	8
24	Din12	Digital Input	0	2	16
25	Din13	Digital Input	0	2	32
26	Din14	Digital Input	0	2	64
27	Din15	Digital Input	0	2	128
28	Dout00	Digital Output	0	9	1
29	Dout01	Digital Output	0	9	2
30	Dout02	Digital Output	0	9	4
31	Dout03	Digital Output	0	9	8
32	BP-TD	Backplane Transmit Data			

Connections: (continued)

Terminal	Signal	Description	Subslot	Register	Mask
33	BP-RD	Backplane Receive Data			
34	PC-RD	Host Computer Receive Data			
35	PC-TD	Host Computer Transmit Data			
36	PC-CTS	Host Computer Clear-to-Send			
37	PC-RTS	Host Computer Request-to-Send			
38	PWM0	Pulse Width Output	0	13	0
39	PWM1	Pulse Width Output	0	14	0
40	PWM2	Pulse Width Output	0	15	0
41	Dout04	Digital Output	0	9	16
42	Dout05	Digital Output	0	9	32
43	Dout06	Digital Output	0	9	64
44	Dout07	Digital Output	0	9	128
45	Dout08	Digital Output	0	10	1
46	Dout09	Digital Output	0	10	2
47	Dout10	Digital Output	0	10	4
48	Dout11	Digital Output	0	10	8
49	Dout12	Digital Output	0	10	16
50	Dout13	Digital Output	0	10	32
51	Dout14	Digital Output	0	10	64
52	- dnc -	Do not connect			
53	- dnc -	Do not connect			
54	- dnc -	Do not connect			
55	- dnc -	Do not connect			
56	- dnc -	Do not connect			
57	- dnc -	Do not connect			
58	RST/	Reset Input			
59	Ain00	Analog Input	0	3	0
60	Ain01	Analog Input	0	4	0
61	Ain02	Analog Input	0	5	0
62	AGnd	Analog Ground			
63	DGnd	Digital Ground			
64	APwr	+3.3 to 3.6V AnalogPower			

Connections: (continued)

The serial communications port provides 4 signals: TD, RD, RTS, CTS in the modem sense. These are low-voltage signals.
In order to connect to an RS-232 port, these signals need to be level-shifted and inverted via a suitable interface such as the industry-standard SN75155.
Alternately, FTDI supply a USB-to-low-level serial interface which will connect directly to the CPDA-99. See http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf for details. The **TTL-232R-3V3-WE** device is the appropriate product: the wire ends need to be attached to a 5-way 0.1" receptacle in the appropriate order to make the connection. **Please do not use the device without the -WE suffix: the connections to the SIL connector are in the wrong order!**

Interface to Diagram:

The Slot address for all facilities is always Slot 0 for a CPDA-99.

Subslot 0: Input/Output

Register 0: Device Identifier: returns hex A502 (42242) for CPDA-99
Register 1: Digital Inputs: bit mapped: use mask to select required input
Register 2: Digital Inputs: bit mapped: use mask to select required input
Register 3: Analog Input 00: returns 0 to 2.50
Register 4: Analog Input 01: returns 0 to 2.50
Register 5: Analog Input 02: returns 0 to 2.50
Register 6: Analog Input 03: returns 0 to 2.50
Register 7: Analog Input 04: returns 0 to 2.50
Register 8: Analog Input 05: returns 0 to 2.50
Note that writing (outputting) to the above registers has no effect

Register 9: Digital Outputs: bit mapped: use mask to select required output
Register 10: Digital Outputs: bit mapped: use mask to select required output
Register 11: Analog Output 00: 0 to 10.00 corresponds to output voltage
Register 12: Analog Output 01: 0 to 10.00 corresponds to output voltage
Register 13: PWM Output 0: 0 to 255 controls pulse width in 125 ns steps.
Register 14: PWM Output 1: 0 to 255 controls pulse width in 125 ns steps.
Register 15: PWM Output 2: 0 to 255 controls pulse width in 125 ns steps.
Register 16: Count14: medium-speed up counter attached to Din14
Register 17: Count15: medium-speed up counter attached to Din15
Register 18: CountQ: medium-speed up/down quadrature counter attached to Din 14 and 15.
Register 19: CountCtrl: Provides reset and hold facilities for the medium-speed counters.
- Mask 1: C14 Reset: Forces Count14 to zero. Once the reset has occurred, the bit itself is reset.
- Mask 2: C14 Hold: Stops Count14 and holds its value. Set and reset via TERMOUT.
- Mask 4: C15 Reset: Forces Count15 to zero. Once the reset has occurred, the bit itself is reset.
- Mask 8: C15 Hold: Stops Count15 and holds its value. Set and reset via TERMOUT.
- Mask 16: CQ Reset: Forces CountQ to zero. Once the reset has occurred, the bit itself is reset.
- Mask 32: CQ Conditional Reset: Forces CountQ to zero when ISW6 and ISW7 are both FALSE (high). Once the reset has occurred, the bit itself is reset. This function is useful where the index signal on a quadrature encoder spans more than one step of the encoder.

Registers 20 through 27: Computer Interface: These registers can be written to by an external computer and read into the diagram. See the Advanced Programmer's Manual for details.

Advanced Programming Capabilities

Advanced programming capabilities are accessible via subslots 1 through 4. These require advanced knowledge of computer interfacing and software. Details are provided in the AmbiLogique Advanced Programmer's Manual, but they are summarised here:

Subslot 1: Readout of Internal Signals

Reg 0 Mask 0:	Signal Refnum (read/write).
Reg 1 Mask 0:	Signal Value (refnum non-preincremented) (read only).
Reg 2 Mask 0:	Signal Value (refnum preincremented) (read only).
| |	
Reg 16 Mask 0:	Signal Value (refnum preincremented) (read only).

Subslot 2: Operating Mode and Communications Statistics

Reg 0 Mask 1:	Operating Mode: 0 = normal; 1 = stopped (read/write).
Reg 1 Mask 255:	Time used in processing diagram: 0 = none; 255 = full slot time allocation (read only).
Reg 2 Mask 0:	Millions of backplane transactions.
Reg 3 Mask 0:	No. of backplane transactions up to 1 million
Reg 4 Mask 0:	No. of backplane transactions in error.
Reg 5 Mask 0:	NoRep count: No Response to BRQ or BCM packet.
Reg 6 Mask 0:	Timeout count: Slave took excessive time to provide complete response.
Reg 7 Mask 0:	SentErr count: Incorrect packet sentinel detected.
Reg 8 Mask 0:	FormErr count: Format of received packet incorrect.
Reg 9 Mask 0:	CWErr count: Checkword of received packet did not compute correctly.

Subslot 3: Constants Memory (User Constants)

Reg 0 Mask 0:	Constant Refnum (read/write)
Reg 1 Mask 0:	Constant Value (refnum non-preincremented) (read/ write occasionally)
Reg 2 Mask 0:	Signal Value (refnum preincremented) (read/ write occasionally)
| |	
Reg 16 Mask 0:	Signal Value (refnum preincremented) (read/ write occasionally)

Subslot 4: Function Block Memory (User Program)

Reg 0 Mask 0:	Func Block Exec number (read/write)
Reg 1 Mask 0:	Func Block Type number (read/ write occasionally)
Reg 2 Mask 0:	Pin 0 Descriptor (read/ write occasionally)
| |	
Reg 16 Mask 0:	Pin 16 Descriptor (read/ write occasionally).

Subslot 255: Firmware Revision Level

Reg 0 Mask 0: Firmware Revision

(Major_revision * 256) + minor_revision.
Example: Rev 3.20 => (3 * 256) + 20 = 788.
Easily decoded as a hexadecimal number:
788d = 314h => 300h + 14h => 3.20

Specifications

1. Power Input:
   +3.3 to 3.6 V 50 mA

2. Digital Inputs:

FALSE voltage:	2.0 to 3.6 V
TRUE voltage	0.0 to 0.6 V
Sink /source current:	not greater than 1.0 µA
Maximum Input voltage:	-0.1 to +3.5 V
Protection:	None: external protection MANDATORY

3. Analogue Inputs:

Resolution:	12 bits: 610 µV per bit
Range:	0 to 2.5 V
Input resistance:	not less than 1 MÙ
Total errors not exceeding:	4 bits: 2.5 mV: 0.12 % of full range
Protection:	None: external protection MANDATORY

4. Digital Outputs:

Max working voltage:	+ 3.6 Vdc
Max current:	10 mA individually: total for all outputs not to exceed 20mA
Protection:	None: external protection MANDATORY

5. Analogue Outputs:

Resolution:	10 bits : 2.4 mV per bit
Range:	0 to 2.5 V
Max Output Current:	1 mA
Total errors not exceeding:	4 bits : 10 mV : 0.25 % of full range
Protection:	None: external protection MANDATORY

6. Scan Rate — 16 Hz (62.5 ms)

7. Diagram Capacity — 250 Function Blocks of any type

8. Dimensions:

Height:	20 mm above mother board
Width:	59 mm max
Depth:	59 mm max

9. Ambient temperature: — -10 to +60 °C

WARNING
SAFETY-CRITICAL SYSTEMS

A Safety-Critical system is a system whose failure or malfunction could cause death, significant injury or loss of property.

AmbiLogique products incorporate electronic hardware and software, both of which carry a remote but real possibility of failure. AMBILOGIQUE DOES NOT WARRANT, CLAIM OR REPRESENT THAT ITS PRODUCTS ARE INFALLIBLE.

It is therefore THE RESPONSIBILITY OF THE DESIGNER of any safety-critical system which incorporates AmbiLogique products to ensure that:-

1. The system is designed so that any failure of an AmbiLogique component will not cause death, injury or loss of property.
2. The system incorporates independent monitoring means which detect the failure of any of the electronic control elements.
3. The system has alternative and independent means of control which enable it to be controlled and shut down in an orderly manner.
4. Any and all other industry-specific safety requirements are fully implemented.

Revision History:

R 1.0	2010-05-01	Initial Issue
R 2.0	2012-01-25	Open Document format, Name change, ARTPC enhancements added.
R 2.1	2012-01-26	Improved graphics.